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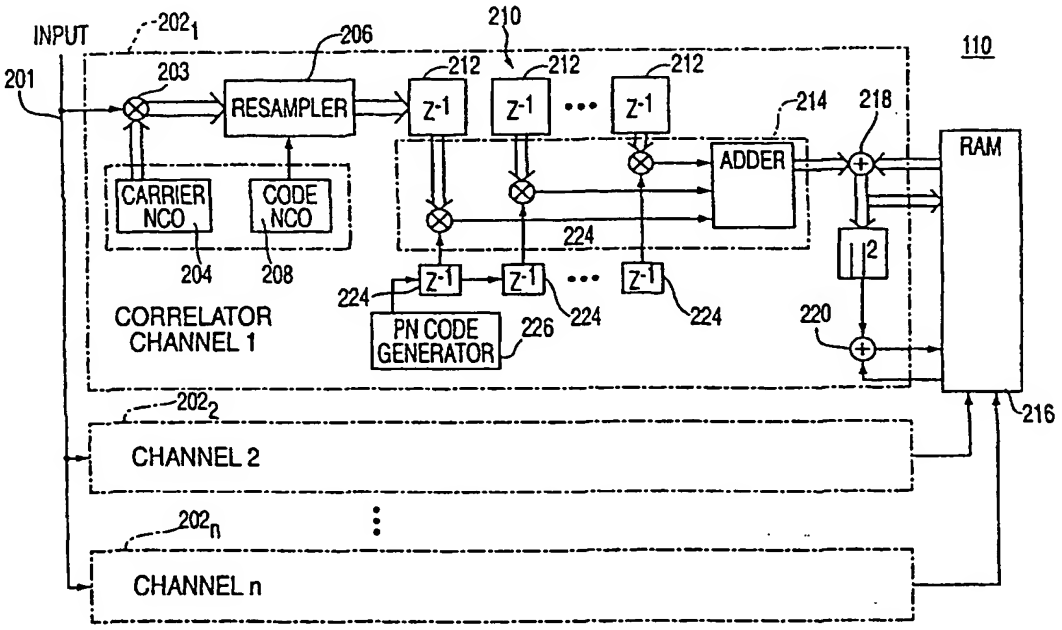
(54) Title: APPARATUS FOR COMPUTING GPS CORRELATIONS IN PARALLEL



(57) Abstract

The invention provides apparatus (110) for rapidly acquiring GPS signals. The apparatus (110) is suitable for implementation in custom digital logic, for example, within an application specific integrated circuit (ASIC). The apparatus (110) consists of several channels (202) of processing circuity, each intended to detect and make signal measurements from a particular GPS satellite that is in view of the receiver.

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APPARATUS FOR COMPUTING GPS CORRELATIONS IN PARALLEL

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/130,882, filed April 23, 1999, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention relates to signal processing in global positioning system (GPS) receivers. In particular, the present invention relates to an apparatus for performing many GPS correlations in parallel so as to enhance the performance of a GPS receiver.

2. Description of the Background Art

Many emerging applications of GPS require receivers that are capable of acquiring signals rapidly and in difficult signal environments. For example, system requirements may dictate that a system obtain a GPS position in a few seconds, and be able to operate in areas where the received GPS signals are weak and unstable, for example, inside buildings and in urban "canyons".

Conventional GPS receivers typically utilize one or two programmable correlators to acquire and track each GPS signals. When searching for signals, the correlator is used in a sequential manner to examine all possible timings on an incoming satellite PN code. In order to detect weak signals, a significant dwell time for averaging is required when examining each signal timing. Since the different timings are evaluated sequentially, the dwell times are cumulative, resulting in lengthy acquisition times.

Because of this limitation, such conventional receivers cannot be used to quickly detect weak signals.

Therefore, there is a need in the art for a correlator that rapidly acquires GPS signals.

SUMMARY OF THE INVENTION

The invention provides apparatus for rapidly acquiring GPS signals. The apparatus is suitable for implementation in custom digital logic, for example, within an application specific integrated circuit (ASIC). The apparatus consists of several channels of processing circuitry, each intended to detect and make signal measurements from a particular GPS satellite that is in view of the receiver.

The apparatus is intended to serve as a processing element within a complete GPS receiver. In particular, the apparatus processes samples of a down-converted intermediate frequency (IF) waveform, such as would be produced by a conventional GPS antenna and radio frequency (RF) front end. The apparatus is intended to integrate to a DSP or general purpose microprocessor which implements standard GPS functions such as control, measurement processing, and position computation.

The apparatus performs a large number of GPS correlations in parallel for each channel. Furthermore, the apparatus comprises an accumulator for averaging such correlations over long dwell times so that weak signals may be detected. A significant feature of the approach is that a large number of correlation results are made available concurrently, thus eliminating or greatly reducing the need to perform sequential search operations.

When coupled with other elements to form a complete GPS processing system, the apparatus provides the ability

to rapidly acquire GPS signals even at low signal levels where long averaging times are required.

BRIEF DESCRIPTION OF DRAWINGS

The teachings of the present invention may be readily understood by considering the following detailed description in conjunction with the accompanying drawing, in which:

FIG. 1 depicts a functional block diagram of a GPS receiver;

FIG 2. depicts a block diagram of the apparatus of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 depicts a GPS satellite constellation 102 and a GPS receiver 106. The constellation 102 comprises a plurality of satellites that continuously transmit GPS signals to the receiver 106. The receiver 106 comprises an antenna 104, a GPS front end 108, a GPS signal processor 110 and a controller 112. The antenna 104 simultaneously receives GPS signals from a plurality of satellites. The GPS front end 108 downconverts the received signal to an intermediate frequency (IF). The IF signal is coupled to the GPS signal processor 110. The present invention is a portion of the processor 110. The receiver 106 is controlled by controller 112.

The process of acquiring a GPS signal centers around the need to search for signals in the presence of noise and/or interference. Generally, the search process involves two parameters. First, a search must be conducted

in the frequency domain, to examine all possible frequency offsets between the local GPS receiver frequency reference and the frequency of the incoming signal. Second, a search must be conducted in the time domain to examine all possible signal delays between the local GPS time reference and the timing of an incoming signal.

Multiple error sources contribute to the frequency uncertainties giving rise to the need for search over frequency. First, depending on the context in which the search is being conducted, there may be relatively little information available regarding the satellite signals themselves. For example, in a so-called cold start, the GPS receiver is un-initialized with respect to time and position and cannot estimate the positions of the satellites in the sky. In this case, the frequency uncertainty assigned to satellite motion must encompass the full range of Doppler variations. A second source of uncertainty is motion of the mobile receiver, which induces a Doppler shift relative to the incoming signals, also contributing to frequency uncertainty. A final, and often dominant, source of uncertainty is the unknown clock frequency of the GPS receiver.

Furthermore, the timing of the incoming signal is initially unknown in a GPS receiver. The GPS code modulation consists of 1023 chips spanning a one millisecond interval. The starting point of this code relative to the receiver's clock must be determined by searching over all possible timing hypothesis. Typically, the delay uncertainty is searched in a sequential manner by advancing the reference code in one-half chip increments. As mentioned above, if weak signals are to be detected, the receiver must dwell at each timing hypothesis.

The combination of the search in time and frequency can lead to a lengthy overall acquisition process. For example, if 10 frequencies must be checked, at each of 1023 delays, in one-half chip steps, then a total of 20,460 searches must be conducted. Detecting a weak signal can require dwell times for averaging as long as several hundred milliseconds. In this example, if the needed dwell was 200 milliseconds the conventional receiver would need over 4000 seconds to conduct a search.

Recently, GPS architectures have emerged where information from a server is used to help the GPS receiver reduce the frequency uncertainty of searching, and many of these techniques can ensure that at most one frequency band need be searched. Nevertheless, as should be clear from the above example, the code delay search is still very time consuming.

The current invention provides the ability to search many delay hypotheses in parallel. In a preferred embodiment, all delays are searched in parallel. Furthermore, the invention provides a technique for averaging the resulting searches over long dwell times to provide sensitivity for acquiring weak signals. As can be seen, the architecture therefore provides the ability to accelerate the search process by a factor of several thousand. In particular, relating to the example above, if all delays can be searched in parallel, and only one frequency hypothesis need be examined, the invention could complete the search process in a single 200 millisecond dwell.

The operation of the apparatus may best be understood by reference to FIG. 2 which depicts a functional block diagram of the GPS signal processor 110.

The input to the processor is IF input samples 201 from the GPS RF front end 108. The GPS signal processor 110 comprises a plurality of parallel correlator channels 202_i (where i is an integer) and a memory 216. The IF data is distributed among the plurality of correlator channels 202_i, each programmed to search for signals from a particular satellite in view.

In each channel 202, IF input samples 201 are first multiplied by a complex exponential term using a multiplier 203 to remove an IF carrier frequency. The complex exponential is generated by numerically controlled oscillator 204. The NCO frequency is set to the IF frequency, which is composed of a fixed term (due to the design of the RF section), and a carrier frequency correction term due to doppler. The multiplication step generates a complex result, i.e., the result is composed of an in-phase term (generated by mixing with a cosine function of the carrier phase) and a quadrature term (generated by mixing with a sine function of the carrier phase). In FIG. 2, for clarity, the flow of complex values with in-phase and quadrature components is represented by double-lined arrows.

The carrier-corrected samples are re-sampled using a resampler 206 in order to yield samples at the desired input rate for the correlation process. In one embodiment, the resampler 206 is implemented as an integrate and dump circuit which periodically provides a pre-summed value to the parallel correlator. The dump event of the resampler 206 is controlled by a second NCO 208 that generates a sample signal that properly distributes the chips of the incoming PN modulation across the parallel correlator. The NCO value is programmed based on the expected code rate of the incoming signal. It should be noted that this code

rate has a fixed 1/1540 relationship to the carrier frequency Doppler.

The digital circuit runs on a single clock, such that the time interval of an individual integration in resampler 206 will always begin and end on a clock cycle. On an instantaneous basis, this introduces variations in the sample timing relative to the incoming PN code. These variations, however, cause only slight changes in the overall correlation process because the NCO will, on average, generate the correct sample timing.

The output of the resampler 206 passes to the core correlators 210 that perform the tasks of calculating the convolution between the received signal and a set of reference waveforms for each satellite in view. Each parallel correlator 210 comprises a plurality of delay units 212 a large multiply-and-add logic block 214 that computes the correlation between a full epoch worth of input data 201 and the complete pseudo noise code sequence for the desired satellite. On each clock cycle, a new correlation result for a particular input signal delay is generated and stored in random access memory (RAM) 216. After a full millisecond of clock cycles, the RAM 216 will contain a complete set of correlation results for all delays. This array of results is the convolution between the input signal 201 and the reference waveform.

In one embodiment, eight parallel correlator channels 202 are used, allowing simultaneous sensing of up to eight satellites in view. The size of each correlators 210 within each channel 202 depends on the granularity required in the convolution result. A 2046-wide parallel correlator 210 provides convolution results spaced at intervals 1/2 PN code chip. This is adequate to detect and estimate the

location of the true peak correlation, which in general falls between bins of the convolution.

The parallel correlator 110 is designed to detect and measure extremely weak signals. Due to noise, interference, and cross correlation effects these low signal levels are not detectable through analyzing a single epoch of data. To enhance sensitivity, the block search hardware integrates the results from hundreds of individual convolutions to generate a single composite convolution with improved signal to noise characteristics. Two types of averaging are performed coherent averaging incoherent accumulator 218 and non-coherent averaging in non-coherent accumulator 220.

Coherent averaging offers the ability to greatly enhance the ability to detect correlation peaks in the averaged convolution result. In practice, however, the length of time over which coherent averaging can be used is limited by periodic phase transitions from the GPS data bits.

Non-coherent averaging consists of combining of the complex magnitude of the convolution results. This process also enhances the ability to detect correlation peaks, but unlike coherent average, is insensitive to phase transitions and can be used over longer averaging periods.

Coherent averaging is implemented by directly summing the results of multiple convolutions and using the RAM to store intermediate results. As each correlation is computed, the result is added to an ongoing summation in the RAM for that delay value. At the conclusion of the coherent averaging interval the RAM holds a composite convolution result. One embodiment uses a 9 epoch coherent averaging period (an epoch meaning a full cycle of the PN code). This value is chosen to be significantly smaller

than the average time between data bit transitions. Furthermore the value is chosen so as to randomize the coherent averaging windows against the 20 epoch period of the data bits. In this manner, data bit transitions will have minimal affect on the coherent averaging process.

To further extend the averaging time, non-coherent averaging used. Non-coherent averaging consists of summing the complex magnitudes of the individual convolution results to yield a composite result with improved signal to noise characteristics. The non-coherent averaging process builds upon the results of coherent averaging. As each coherent averaging interval ends, the resulting coherent average is magnitude-squared summed with an ongoing non-coherent averaging value stored in RAM. This process runs for the desired total averaging interval, for example one second. At the end of the process, the complete averaged convolution result will be in RAM and can be accessed by a DSP or general purpose microprocessor that interfaces with the hardware correlator.

Before processing begins, each parallel correlator must be pre-loaded with the reference waveform. There are many possible ways to achieve this preloading. The waveforms for all 32 PN codes, for example, could be stored in hardware and selected via a multiplexer. Alternatively, the reference waveform could be stored in a microprocessor ROM (within controller 112 of FIG. 1) and loaded into the hardware at run time. In another embodiment, the reference waveform is synthesized on the chip by including a numerically controlled oscillator (NCO) 204 and PN code generator 226 that produces samples of the reference waveform. During initialization of the parallel correlator, this reference waveform is clocked in using delay units 224. A single shared NCO 206 and PN code

generator 226 can be used to load all eight correlators in sequence.

It should also be noted that it is not a requirement that the parallel correlator contain processing sufficient to generate the entire convolution. To reduce the hardware complexity, a subset of the convolution results could be processed. In this case, a total search of all PN code delays would require using the parallel correlator several times to compute different portions of the convolution. While this would increase the time to search signals, it should be clear that there is still a great improvement over the single correlator structure used in conventional GPS receivers.

The Block Search implementation described is one particular embodiment. As with many hardware signal processing systems a broad array of hardware implementations are possible.

Although various embodiments which incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

What is claimed is:

1. A satellite-based position location system signal processor comprising:

a plurality of parallel channels for simultaneously correlating a plurality of received signals.

2. The processsor of claim 1 wherein each of said parallel channels comprises:

a multiplier for multiplying a received signal with an oscillator signal;

a resampler for resampling said multiplied signal; and

a correlator coupled to said resampler.

3. The processor of claim 2 wherein said correlator comprises:

a plurality of delay units;

a multiply and add module coupled to said delay units;

a non-coherent accumulator coupled to said module;

a coherent accumulator coupled to said module; and

a memory coupled to said accumulators.

4. The processor of claim 1 wherein a pseudo-noise code reference generator is coupled to each of the plurality of parallel channels.

5. The processor of claim 2 wherein said oscillator signal is generated by a numerically controlled oscillator.

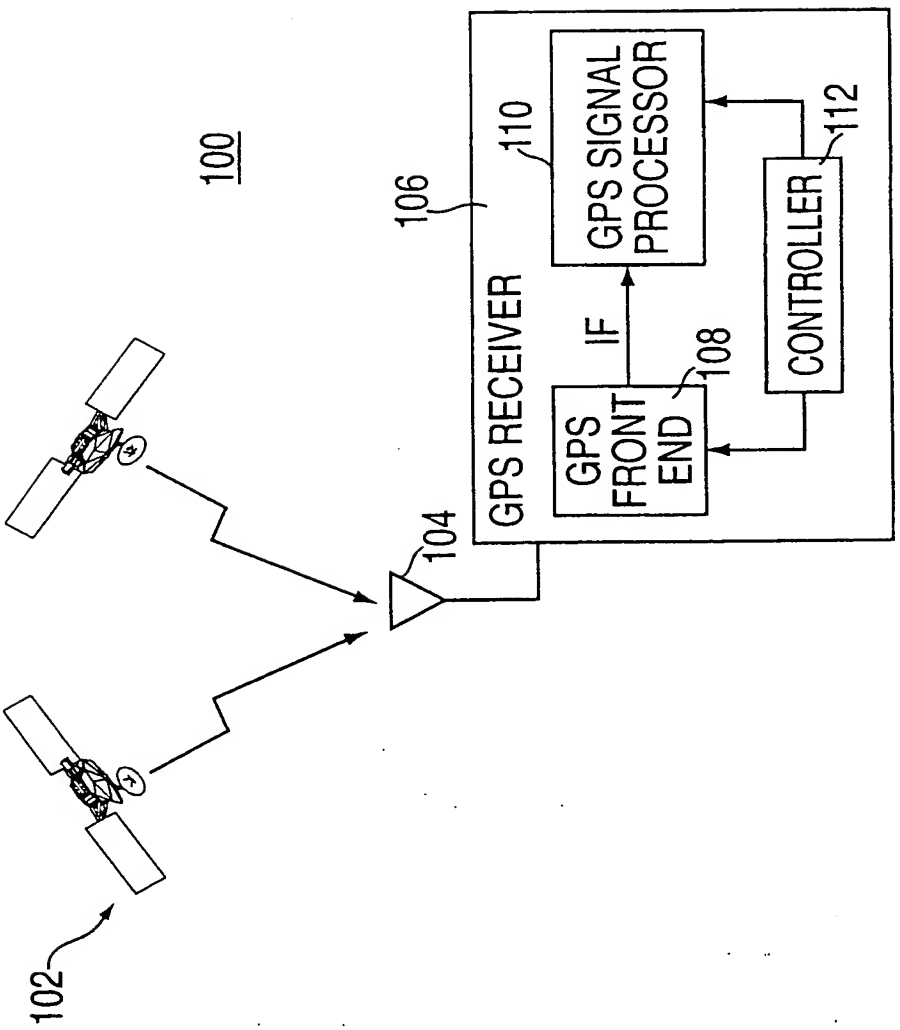
100
102
104
106
GPS RECEIVER
110
GPS SIGNAL PROCESSOR
112
CONTROLLER
IF
108
GPS FRONT END

FIG. 1

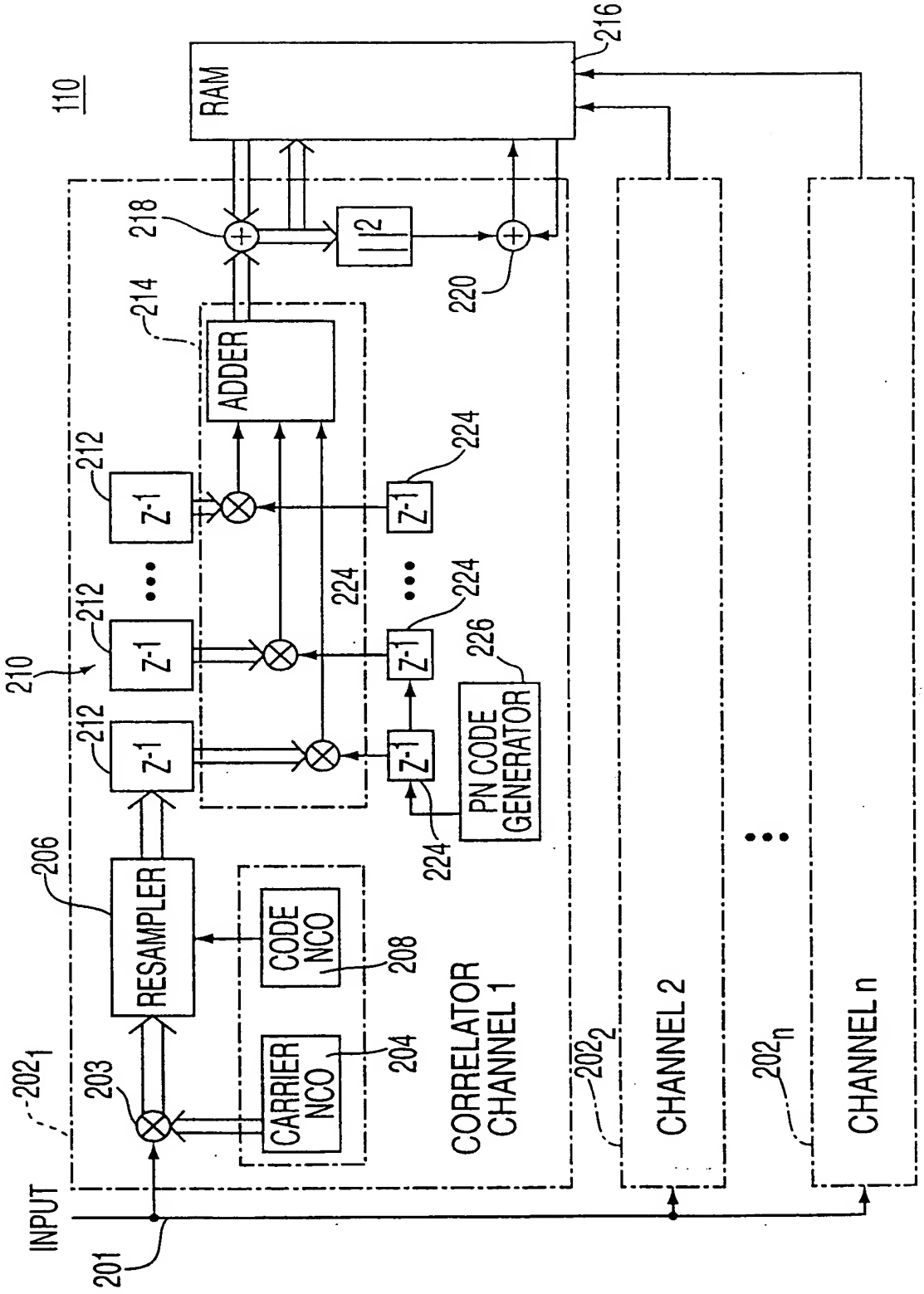
110
RAM
216
218
220
214
ADDER
212
224
210
226
PN CODE GENERATOR
206
RESAMPLER
CODE NCO
208
CARRIER NCO
204
203
202_1
CORRELATOR CHANNEL 1
202_2
CHANNEL 2
202_n
CHANNEL n
INPUT
201

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No. PCT/US00/11020

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H04B 7/185; G06J 1/00; G06F 17/15

US CL :370/290, 320, 335, 342, 441, 479; 375/130, 142, 150, 343

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/290, 320, 335, 342, 441, 479; 375/130, 142, 150, 343

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,896,304 A (TIEMANN ET AL) 20 APRIL 1999, FIGS. 4-6, col. 10, line 12 to col. 14, line 47.	1-5

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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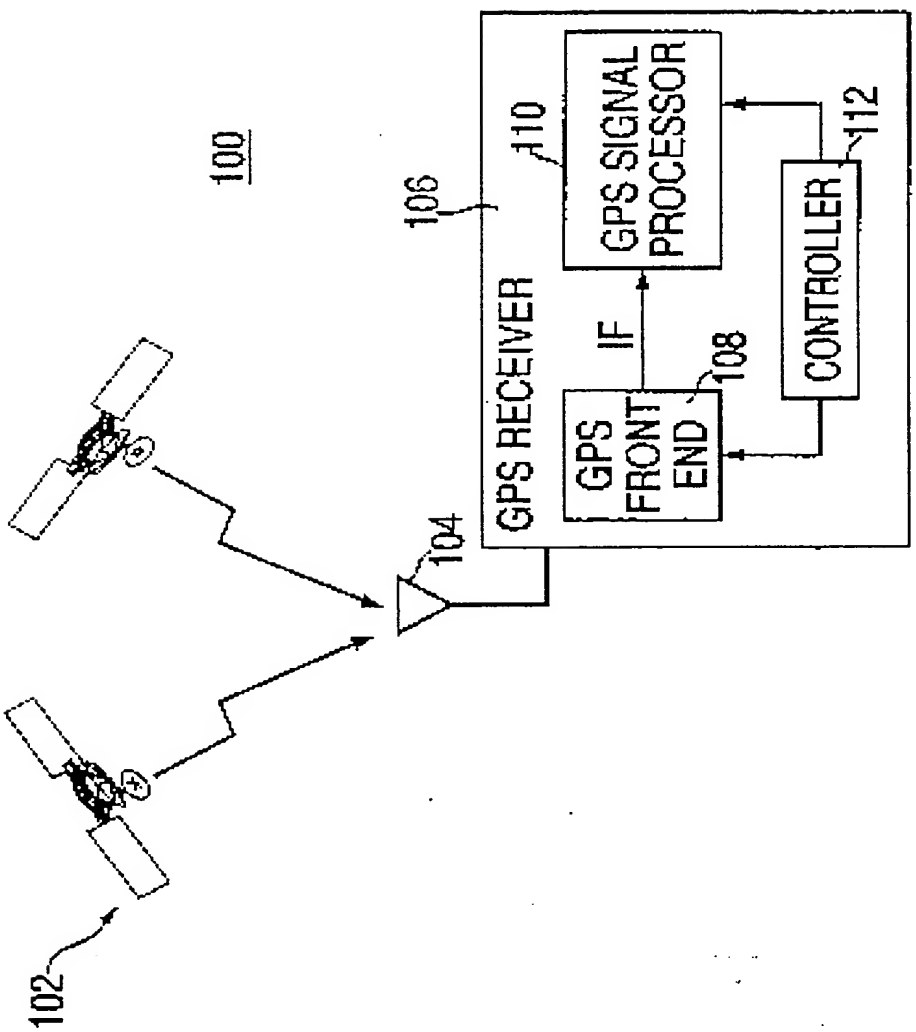
Form PCT/ISA/210 (second sheet) (July 1998)*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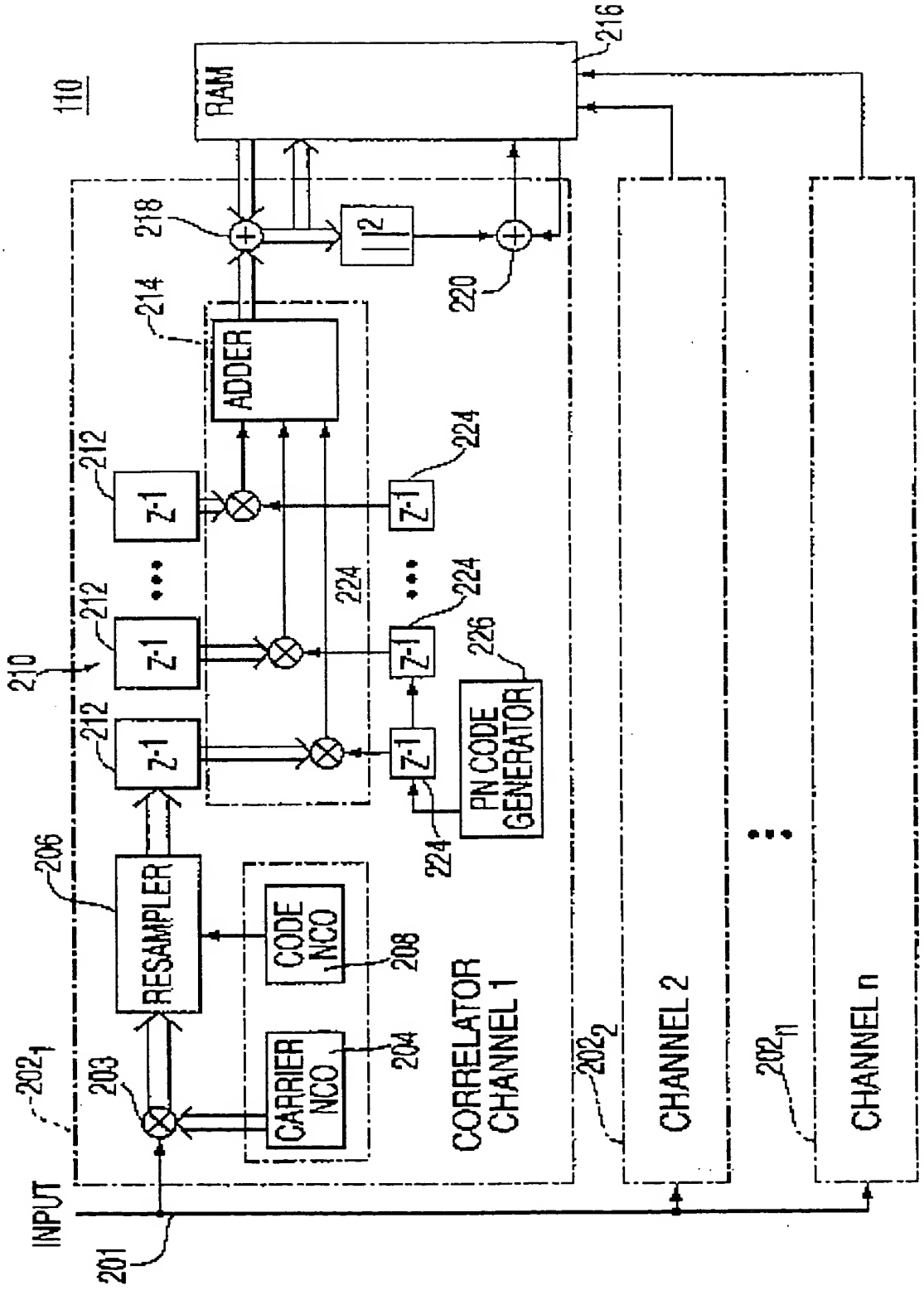
104
106
GPS RECEIVER
110
GPS SIGNAL PROCESSOR
IF
GPS FRONT END
108
CONTROLLER
112

FIG. 1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RESAMPLER
CODE NCO
208
CARRIER NCO
204
203
202_1
INPUT
201
CORRELATOR CHANNEL 1
PN CODE GENERATOR
226
202_2
CHANNEL 2
202_{11}
CHANNEL n

FIG. 2